

# High Step-up SEPIC Converters Based on a Family of Coat Circuit

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**Abstract**—A family of coat circuits for SEPIC converters to improve their boost capability is presented. The present coat circuit does not contain any active switches, so the voltage conversion ratio of the presented converters can be enhanced without complicating its gate driver and control circuits. Meanwhile, because of the expansibility of the coat circuit, the number of its basic cells can be adjusted regarding the actual application requirements. Moreover, in comparison with a conventional SEPIC converter, voltage stress on power switch and diodes of the presented topology is lower at the same output voltage, and thus semiconductor components with low on-resistance are chosen to improve conversion efficiency of converter. The operational principle and steady state analysis of the SEPIC converter with one of the proposed coat circuits have been discussed in detail, and a 300W laboratory prototype is implemented to prove the theoretical analysis of presented converter.

**Index Terms**—Coat circuit, high voltage gain, low voltage stress, SEPIC converter.

## I. INTRODUCTION

IN the past few years, renewable and clean energy like photovoltaic (PV) panels and fuel cells (FC) are becoming more prevalent at the background of the increasing fossil energy consumption [1]–[4]. However, these energy sources usually supply DC voltage with low amplitude like 30–50 V, which makes a DC/DC converter with high boost capacity necessary to step up their output voltage for some applications, like grid integration and hybrid electric vehicles. Affected by parasitic parameters in components and Printed Circuit Board (PCB), the voltage step-up ability of conventional boost converters is limited. Therefore, a conventional boost converter is no longer a good choice for PV and FC sources at the demand of large voltage transfer ratios [5]–[8].

Recently various DC/DC converters with high voltage gain have been presented to step up output voltage. Transformer and coupled inductor with large turn ratios are used to acquire large voltage transfer ratios with different kinds of basic DC/DC converters [9]–[13], however, leakage inductors of the

transformer or coupled inductor result in large voltage stress on active switches and conversion efficiency reduction. To solve this problem, clamping circuits have been adopted in these kinds of converters, which may lead to complexity of the circuit structure and control scheme. By cascading two or more staged boost circuits, high step-up voltage gain can be acquired. These converters have the main drawbacks of complex structure and difficult control. In addition, stability of cascaded converters is poor [14]–[16]. In [17], [18], these presented buck-boost converters have features of single switch, high step-up voltage gain, simple structure and easy control, but discontinuous input current and low-power applications are disadvantages of the converters. To overcome these disadvantages, a quadratic buck-boost converter with a single switch and continuous input current is presented in [19]. The voltage conversion ratio of the converter is the square of that of a conventional buck-boost converter. But the voltage stress of active components is much higher than output voltage. In [20], [21], converters with voltage multiplier (VM) cells have been presented to acquire large voltage conversion ratios and low voltage stress by adding VM cells, thus these converters can increase flexibility in device selection, but in proposed converters, many power switches are used so more drivers are needed and conduction loss is high. Converters with high boost ability based on expandable diode-capacitor VM cells utilize two main switches; there are common advantages like easy control and low input current ripple. But high current stress on capacitors cannot be eliminated [22]–[24].

Generally, continuous low input current ripple is a crucial characteristic in renewable and clean energy applications like PV power generation and FC systems, which improves efficiency and dynamic performance of the systems. Because the inductor is located at the input port of conventional SEPIC converter, the input current ripple of this type of converter can be reduced as inductance increases. SEPIC based converters with continuous input current integrating couple inductor are observed in [25], [26]. By increasing inductor winding turn ratio can greatly improve voltage conversion gain. However, high voltage spike exists in switches and thus an auxiliary snubber circuit is needed. High step-up SEPIC-based converters without coupled inductors has been presented in [27]. Nevertheless, in this converter, active switches suffer high voltage stress and conversion efficiency is low. In [28], a new SEPIC based converter with low voltage stress across power switches and diodes is discussed; its voltage transfer ratio is three times as much as a conventional SEPIC converter. But its structure cannot be expanded, thus the high step-up capacity

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is still limited. With development of industrial technology in recent years, high switching frequency and high-power density have been a main development trend in application of DC/DC converters. A modified step-up SEPIC circuit is presented in [29] which is implemented with a gallium nitride (GaN) device. The presented converter is operated in 1 MHz. With switching frequency increasing, the volume of passive components in the converter decreases, thus overall volume of the converter decreases. But its voltage gain is still not high.

Diverse types of coat circuits for traditional DC/DC converters to achieve large voltage transfer ratio have been presented in [30]. High voltage gain, single active switch, low device voltage stress, and extendibility of the topology are the advantages of these converters. But as to the presented coat circuit-based converters, high voltage and current stresses on the capacitors are the main shortcomings, which restrain the design flexibility and applicability of the types of converters. Therefore, in this paper, other modified coat circuits for conventional DC/DC converters are derived to achieve lower voltage and current stresses on the capacitors, and the SEPIC converter with the optimized coat circuit structure has been

taken as an example to analyze. Furthermore, by using GaN MOSFET, power density of the presented converter is greatly increased. This paper is presented as follows. The general topology configurations and the operational principle are expressed in Section II. Comprehensive performances of the presented converter are discussed in Section III. Experimental results are given in Section IV. Power dissipation analysis is discussed in Section V. The conclusion is provided in Section VI.

## II. PRESENTED TOPOLOGY AND OPERATIONAL PRINCIPLE

The presented family of general SEPIC converter topologies is shown in Fig. 1. All of these SEPIC converters consist of a basic SEPIC converter and coat circuit based on the basic cells. The number of basic cells can be adjusted according to actual application demand. Fig. 1(a) shows a SEPIC converter with coat circuit in [30]. To distinguish it from other topologies in this paper, the converter is called SEPIC-CI. By changing the connection of capacitor  $C_{12}$ ,  $C_{22}$ , and  $C_{n2}$  in coat circuit, a modified SEPIC circuit is presented in Fig. 1(b). For simplification, this converter with a second version of coat

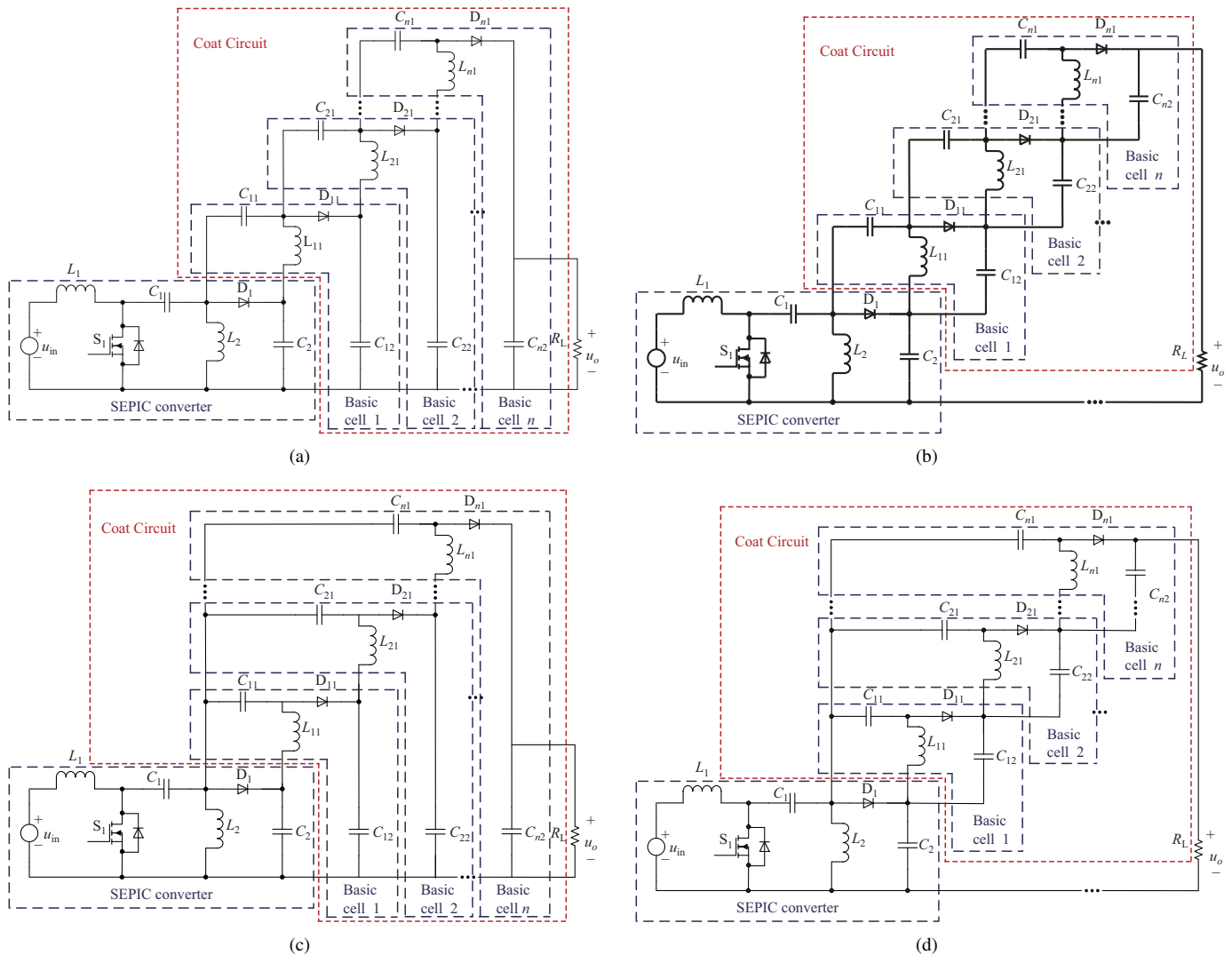


Fig. 1. Topologies of the general SEPIC converters. (a) SEPIC-CI. (b) SEPIC-CII. (c) SEPIC-CIII. (d) SEPIC-CIV.

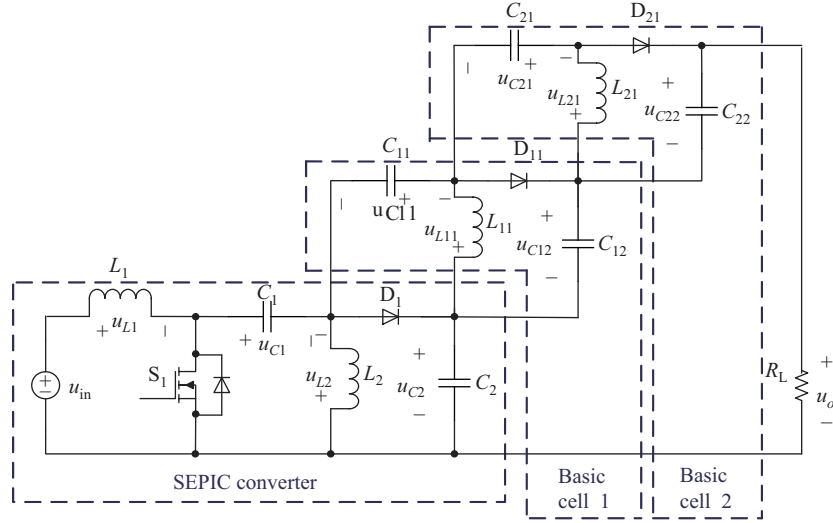


Fig. 2. Topology structure of presented SEPIC-TBC converter.

circuit is named as SEPIC-CII which obtains lower voltage stress across each capacitor compared to SEPIC-CI. Similar to the SEPIC-CII converter, a third version of coat circuit-based SEPIC (called by SEPIC-CIII) converter is given in Fig. 1(c). This converter has the main feature of lower current stress across each capacitor compared to SEPIC-CI converter. Based on the SEPIC-CII converter and SEPIC-CIII converter, the fourth version of coat circuit based SEPIC (called by SEPIC-CIV) converter is also presented in Fig. 1(d).

For better understanding of the operating principle of presented general SEPIC converters, the SEPIC-CII converter with two basic cells (SEPIC-TBC) is taken as an example to analyze the operating principle, as shown in Fig. 2. Assumptions are given for the following analysis: 1) All components are considered ideal and parasitic parameters are negligible; 2) Capacitor value of presented converter is treated as large enough, thus voltage ripple on the capacitors is neglected.

#### A. Continuous Conduction Mode

The SEPIC-TBC converter can operate both in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) as the load  $R_L$  changes. The CCM condition contains two operating states, related voltage and current waveforms of the presented converter operating in CCM are depicted in Fig. 3.  $D$  represents the duty cycle of the switch  $S_1$ , ranging from 0 to 1. Other voltage or current variables are labeled in Fig. 4 and 6. The analysis process is given as follows.

First state  $[t_0 - t_1]$ : In this state, switch  $S_1$  conducts, diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  turn OFF, and corresponding circuit is given in Fig. 4(a). The inductor  $L_1$  is magnetized by the input voltage source  $u_{in}$ , the inductor  $L_2$  is magnetized by the capacitor  $C_1$ , the inductor  $L_{11}$  is magnetized by the capacitor  $C_1$  and  $C_2$ , the inductor  $L_{21}$  is magnetized by the capacitor  $C_1$ ,  $C_2$ , and  $C_{12}$ , all inductor current rises linearly. Capacitor  $C_{11}$  is charged by capacitor  $C_1$  and  $C_2$ , the capacitor  $C_{21}$  is charged by the capacitor  $C_1$ ,  $C_2$ , and  $C_{12}$ , capacitor  $C_1$ ,  $C_2$ ,  $C_{12}$ , and  $C_{22}$  are discharged. Voltages across all inductors can be written as

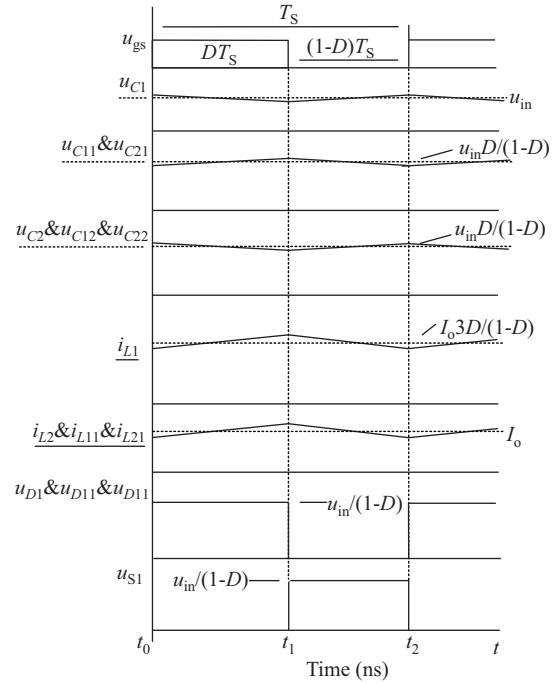


Fig. 3. Related waveforms of the SEPIC-TBC converter operating in CCM.

$$\begin{cases} u_{L1} = u_{in} \\ u_{L2} = u_{C1} \\ u_{L11} = u_{C2} + u_{C1} - u_{C11} \\ u_{L21} = u_{C12} + u_{C2} + u_{C1} - u_{C11} - u_{C21} \end{cases} \quad (1)$$

Second state  $[t_1 - t_2]$ : At time  $t_1$ , switch  $S_1$  turns OFF, diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  conduct, and the corresponding circuit is given in Fig. 4(b). The current of inductor  $L_1$  flows through capacitor  $C_1$  then branches off through three paths. The first passes through diode  $D_1$  to capacitor  $C_2$ , the second passes through capacitor  $C_{11}$  and diode  $D_{11}$  to capacitor  $C_2$  and  $C_{12}$ , the third passes through capacitor  $C_{11}$  and  $C_{21}$  and diode  $D_{21}$  to capacitor  $C_{22}$ ,  $C_{12}$ , and  $C_2$  and load  $R_L$ . Current of inductor  $L_2$  passes through diode  $D_1$  to capacitor  $C_2$ ,

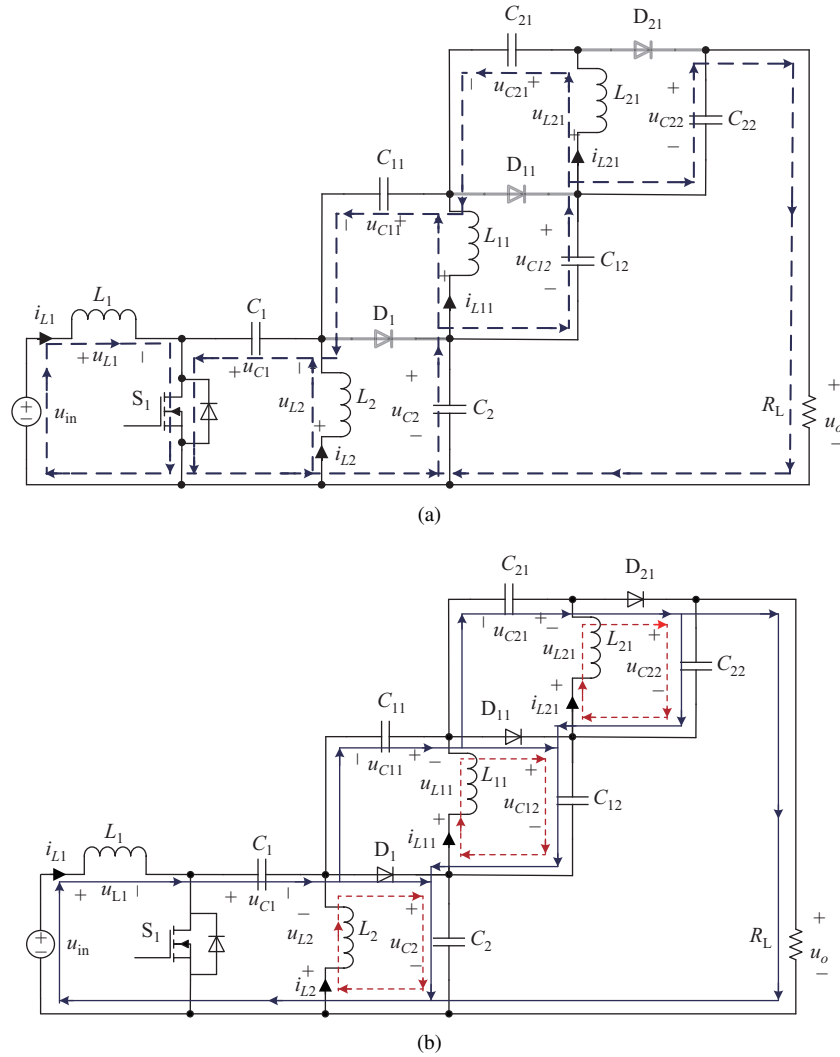


Fig. 4. Corresponding circuits of the SEPIC-TBC converter operating in CCM. (a) First state. (b) Second state.

current of inductor  $L_{11}$  passes through diode  $D_{11}$  to capacitor  $C_{12}$ , current of inductor  $L_{21}$  passes through diode  $D_{21}$  to capacitor  $C_{22}$  and load  $R_L$ . All inductor currents descend linearly, capacitor  $C_{11}$  and  $C_{21}$  is discharged, capacitor  $C_1$ ,  $C_2$ ,  $C_{12}$ , and  $C_{22}$  are charged. The related expression can be given by

$$\begin{cases} u_{L1} = u_{in} - u_{C1} - u_{C2} \\ u_{L2} = -u_{C2} \\ u_{L11} = -u_{C12} = -u_{C11} \\ u_{L21} = -u_{C22} = -u_{C21} \end{cases} \quad (2)$$

The operational principle of the SEPIC-CIII converter and SEPIC-CIV converter is alike so SEPIC-CII converter here is not discussed. Comparative properties of the family of general SEPIC converters are listed in Table I.

#### B. Discontinuous Conduction Mode

For simplifying the analysis process of presented SEPIC-TBC converter operating in DCM, we assumed that  $L_1 = L_0$ ,  $L_2 = L_{11} = L_{21} = L$ . Operation of presented converter in DCM consists of five states, related waveforms are shown in

Fig. 5.  $D_M$  represents the proportion of time that the diode is conducting during one switching period. Detailed discussion is explained as follows:

First state  $[t_0 - t_1]$ : At the time  $t_0$ , switch  $S_1$  turns ON, and diodes  $D_1$ ,  $D_{11}$ ,  $D_{21}$  turn OFF. Current  $i_{L1}$  increases linearly, while current  $i_{L2}$ ,  $i_{L11}$ , and  $i_{L21}$  decrease in the negative direction and reach zero at time  $t_1$ . During the time interval, capacitors  $C_1$ ,  $C_2$ , and  $C_{12}$  are charged, the capacitors  $C_{11}$ ,  $C_{21}$ , and  $C_{22}$  are discharged.

Second state  $[t_1 - t_2]$ : Switch  $S_1$  remains ON state, diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  remain OFF state. Currents of all inductors increase linearly. During the time interval, capacitors  $C_1$ ,  $C_2$ ,  $C_{12}$ , and  $C_{22}$  are discharged, the capacitors  $C_{11}$ ,  $C_{21}$  are charged. Switch  $S_1$  turns OFF, diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  conduct at time  $t_2$ .

Third state  $[t_2 - t_3]$ : Switch  $S_1$  is OFF, diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  are ON. Currents of all inductors start decreasing linearly, and current  $i_{L2}$ ,  $i_{L11}$ , and  $i_{L21}$  reach zero at time  $t_3$ . During the time interval, capacitors  $C_1$ ,  $C_2$ ,  $C_{12}$ , and  $C_{22}$  are charged, capacitors  $C_{11}$ ,  $C_{21}$  are discharged.

Fourth state  $[t_3 - t_4]$ : In this state, the corresponding circuit is illustrated in Fig. 6(a), switch  $S_1$  keeps OFF state and

TABLE I  
COMPARATIVE PROPERTIES OF THE FAMILY OF GENERAL SEPIC CONVERTERS

| Topology                        | SEPIC-CI                                                                                                                                                                          | SEPIC-CII                                                                                                                                                 | SEPIC-CIII                                                                                                                                   | SEPIC-CIV                                                                                                                                                                         |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Total device count              | $6 + 4n$                                                                                                                                                                          | $6 + 4n$                                                                                                                                                  | $6 + 4n$                                                                                                                                     | $6 + 4n$                                                                                                                                                                          |
| Voltage gain                    | $\frac{(1+n)D}{1-D}$                                                                                                                                                              | $\frac{(1+n)D}{1-D}$                                                                                                                                      | $\frac{(1+n)D}{1-D}$                                                                                                                         | $\frac{(1+n)D}{1-D}$                                                                                                                                                              |
| Switch and diode voltage stress | $\frac{u_o}{(1+n)D}$                                                                                                                                                              | $\frac{u_o}{(1+n)D}$                                                                                                                                      | $\frac{u_o}{(1+n)D}$                                                                                                                         | $\frac{u_o}{(1+n)D}$                                                                                                                                                              |
| Capacitor voltage stress        | $u_{C1} = u_{in}$<br>$u_{Ci1} = u_{C2} = Du_{in}/(1-D)$<br>$u_{Ci2} = (i+1)Du_{in}/(1-D)$                                                                                         | $u_{C1} = u_{in}$<br>$u_{C2} = u_{Ci1} = u_{Ci2} = Du_{in}/(1-D)$                                                                                         | $u_{C1} = u_{in}$<br>$u_{Ci1} = u_{C(i-1)2} = iDu_{in}/(1-D)$<br>$u_{Cn2} = (n+1)Du_{in}/(1-D)$                                              | $u_{C1} = u_{in}$<br>$u_{Ci1} = iDu_{in}/(1-D)$<br>$u_{Ci2} = u_{C2} = Du_{in}/(1-D)$                                                                                             |
| Capacitor current stress        | $i_{C1(rms)} = (n+1)I_o \cdot \sqrt{D/(1-D)}$<br>$i_{Ci1(rms)} = (n+1-i)I_o \cdot \sqrt{D/(1-D)}$<br>$i_{C(i-1)2(rms)} = I_o \sqrt{D/(1-D)}$<br>$i_{Cn2(rms)} = \Delta i_{Ln1}/4$ | $i_{C1(rms)} = (n+1)I_o \cdot \sqrt{D/(1-D)}$<br>$i_{Ci1(rms)} = i_{C(i-1)2(rms)} = (n+1-i)I_o \cdot \sqrt{D/(1-D)}$<br>$i_{Cn2(rms)} = \Delta i_{Ln1}/4$ | $i_{C1(rms)} = (n+1)I_o \cdot \sqrt{D/(1-D)}$<br>$i_{Ci1(rms)} = i_{C(i-1)2(rms)} = I_o \sqrt{D/(1-D)}$<br>$i_{Cn2(rms)} = \Delta i_{Ln1}/4$ | $i_{C1(rms)} = (n+1)I_o \cdot \sqrt{D/(1-D)}$<br>$i_{Ci1(rms)} = I_o \sqrt{D/(1-D)}$<br>$i_{C(i-1)2(rms)} = (n+1-i)I_o \cdot \sqrt{D/(1-D)}$<br>$i_{Cn2(rms)} = \Delta i_{Ln1}/4$ |

where  $i \in [1, n]$

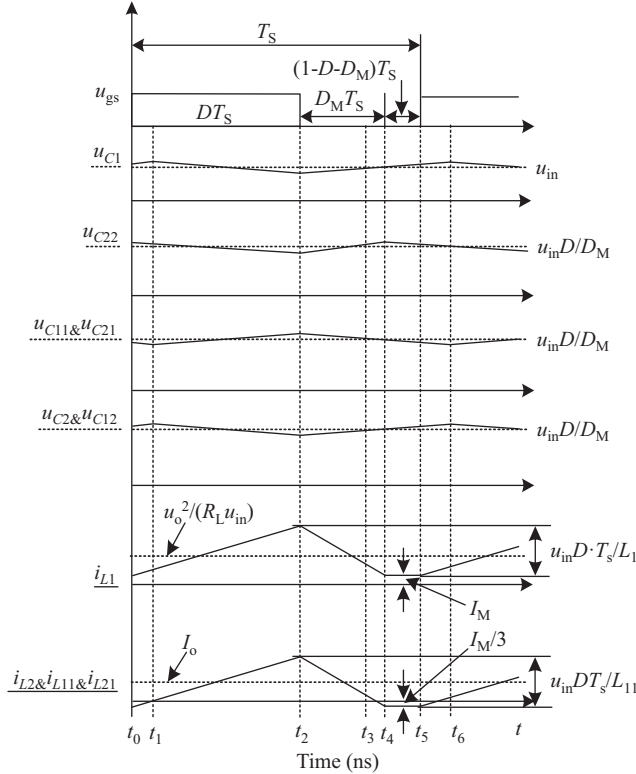


Fig. 5. Related waveforms of the SEPIC-TBC converter operating in DCM.

diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  keep ON state. Current  $i_{L1}$  keeps decreasing linearly, currents  $i_{L2}$ ,  $i_{L11}$ , and  $i_{L21}$  start reversing the direction, as depicted in Fig. 5. The sum of currents of inductors  $L_2$ ,  $L_{11}$ , and  $L_{21}$  are equal to amplitude of current of inductor  $L_1$  at time  $t_4$ , which is marked as  $I_M$ , diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  turn OFF at the end of this duration. During this time interval, capacitors  $C_1$ ,  $C_2$ ,  $C_{12}$ , and  $C_{22}$  are charged, capacitors  $C_{11}$ ,  $C_{21}$  are discharged.

Fifth state  $[t_4 - t_5]$ : In the state, the corresponding circuit

is illustrated in Fig. 6(b), switch  $S_1$  and diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  turn OFF. In this interval time, currents  $i_{L1}$ ,  $i_{L2}$ ,  $i_{L11}$ , and  $i_{L21}$  remain constant. Capacitors  $C_1$ ,  $C_2$ , and  $C_{12}$  are charged, capacitors  $C_{11}$ ,  $C_{21}$ , and  $C_{22}$  are discharged. All modes of this cycle end at time  $t_5$ ; the next cycle will begin and repeat in the same way.

### III. COMPREHENSIVE PERFORMANCE ANALYSIS

#### A. Voltage Gain

According to voltage-second balance principle on all inductors, and by using formulas (1) and (2), voltage on all capacitors of the presented SEPIC-TBC converter operating in CCM can be obtained as follows

$$\begin{cases} u_{C1} = u_{in} \\ u_{C11} = u_{C21} = \frac{u_{in}D}{1-D} \\ u_{C2} = u_{C12} = u_{C22} = \frac{u_{in}D}{1-D} \end{cases} \quad (3)$$

The voltage transfer ratio ( $M_{CCM}$ ) of the presented converter operating in CCM can be calculated by using formula (3).

$$M_{CCM} = \frac{u_o}{u_{in}} = \frac{u_{C22} + u_{C12} + u_{C2}}{u_{in}} = \frac{3D}{1-D} \quad (4)$$

The double-cells of presented SEPIC-TBC converter can also be extended to include  $n$  basic cells, and hence

$$\begin{cases} u_{C1} = u_{in} \\ u_{C11} = u_{C21} = \dots = u_{Cn1} = \frac{u_{in}D}{1-D} \\ u_{C2} = u_{C12} = u_{C22} = \dots = u_{Cn2} = \frac{u_{in}D}{1-D} \\ u_o = u_{C2} + u_{C12} + u_{C22} + \dots + u_{Cn2} = \frac{u_{in}(n+1)D}{1-D} \end{cases} \quad (5)$$

$$M_{CCM} = \frac{u_o}{u_{in}} = \frac{(n+1)D}{1-D} \quad (6)$$

As seen in formulas (5) and (6), the voltage conversion gain of presented SEPIC-CII converter containing  $n$  basic cells is  $n$

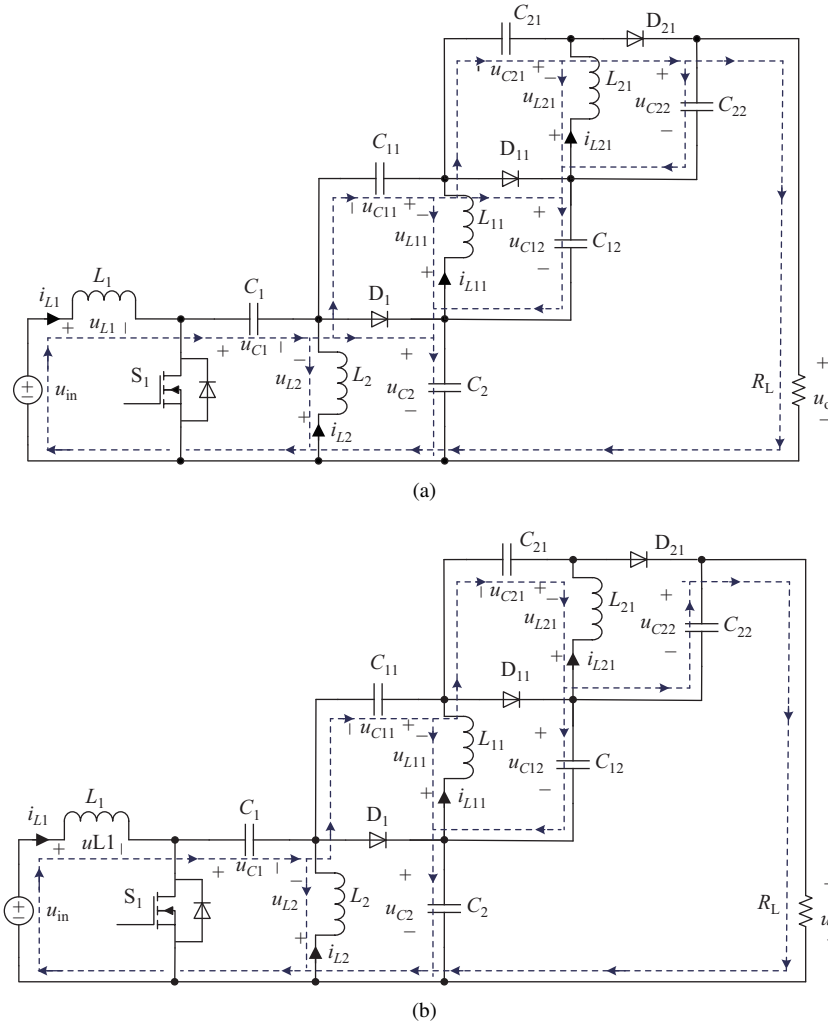


Fig. 6. Corresponding circuits of the SEPIC-TBC converter operating in DCM. (a) Fourth state. (b) Fifth state.

times as large as of traditional SEPIC converter, and its voltage conversion ratio can be changed by adjusting the number of basic cells. Besides, voltage on capacitors of the presented converter is constant and independent of value of  $n$ , which is lower than of the converter of [30]. Therefore, we observed that it is more flexible to select capacitor components in design of converter.

To calculate the voltage transfer ratio ( $M_{DCM}$ ) of presented SEPIC-TBC converter operating in DCM, voltage-second balance principle can be applied on inductors, the voltage of capacitors can be obtained as follows:

$$\begin{cases} u_{C1} = u_{in} \\ u_{C11} = u_{C21} = \frac{u_{in}D}{D_M} \\ u_{C2} = u_{C12} = u_{C22} = \frac{u_{in}D}{D_M} \end{cases} \quad (7)$$

The voltage transfer ratio ( $M_{DCM}$ ) of the presented converter operating in DCM can be obtained as (8) by using formula (7).

$$M_{DCM} = \frac{u_o}{u_{in}} = \frac{u_{C2} + u_{C12} + u_{C22}}{u_{in}} = \frac{3D}{D_M} \quad (8)$$

By applying current-second balance principle on capacitors, the average value of current passing through all diodes and all

inductors is equal to average output current  $I_o$ . Ideally, the presented converter is assumed a lossless system, thus input power is same as out power. Hence, (9) is held. As can be calculated from Fig. 5, the average value of current passing through all inductors is written in (10).

$$\begin{cases} I_{in} = I_{L1} = u_o^2 / (R_L u_{in}) \\ I_{D1} = I_{D11} = I_{D21} = I_{L2} = I_{L11} = I_{L21} = I_o \end{cases} \quad (9)$$

$$\begin{cases} I_{L1} = \frac{u_{in}DT_S}{2L_0}(D + D_M) + I_M \\ I_{L2} = I_{L11} = I_{L21} = \frac{u_{in}DT_S}{2L}(D + D_M) - \frac{I_M}{3} \end{cases} \quad (10)$$

According to (8)–(10), voltage conversion gain of presented converter operating in DCM can be obtained as (11).

$$M_{DCM} = \frac{u_o}{u_{in}} = \sqrt{\frac{(L + 3L_0)R_LD^2T_S}{2L_0L}} \quad (11)$$

Then, we can define dimensionless parameter  $\tau$  as follows:

$$\tau = \frac{2L_0L}{(L + 3L_0)R_LT_S} \quad (12)$$

Substitution of (12) into (11) yields

$$M_{DCM} = \frac{u_o}{u_{in}} = \frac{D}{\sqrt{\tau}} \quad (13)$$

The double-cells of presented SEPIC-TBC converter can be extended to include  $n$  basic cells, and hence

$$M_{DCM} = \frac{u_o}{u_{in}} = \sqrt{\frac{R_L D^2 T_S (L + (n+1)L_0)}{2L_0 L}} \quad (14)$$

The curves of voltage gain versus duty ratio are depicted in Fig. 7, when presented SEPIC-TBC converter operates in CCM condition and in DCM condition under various  $\tau$ , it can be seen that voltage gain  $M_{DCM}$  will increase as  $\tau$  decreases.

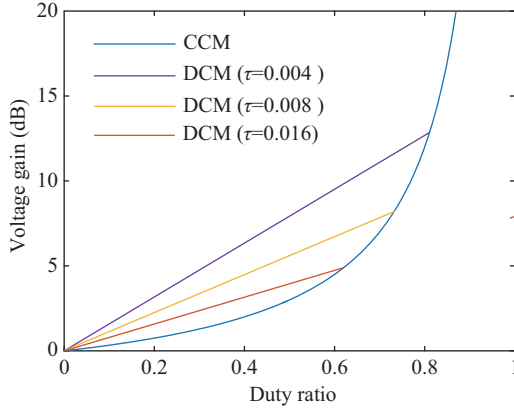


Fig. 7. Voltage gain versus duty ratio.

### B. Voltage and Current Stress Analysis

Voltage stress on switch  $S_1$  and diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  of the presented SEPIC-TBC converter operating in CCM can be given in the following equation by using (3).

$$\begin{cases} u_{S1} = u_{D1} = u_{C1} + u_{C2} = \frac{u_{in}}{1-D} \\ u_{D11} = u_{C12} + u_{C2} + u_{C1} - u_{C11} = \frac{u_{in}}{1-D} \\ u_{D21} = u_{C22} + u_{C12} + u_{C2} + u_{C1} - u_{C11} - u_{C21} = \frac{u_{in}}{1-D} \end{cases} \quad (15)$$

When a basic cell is expanded to  $n$ , the voltage stress can be written as the following formula with (5).

$$u_{S1} = u_{D11} = u_{D21} = \dots = u_{Dn1} = \frac{u_{in}}{1-D} = \frac{u_o}{(1+n)D} \quad (16)$$

As expressed by (16), the voltage of switch and all diodes of presented SEPIC-CII converter with  $n$  basic cells is  $1/(1+n)D$  times smaller than output voltage  $u_o$ , which is much lower than of a traditional SEPIC converter under the same output voltage  $u_o$ , and thus semiconductor devices with low on-resistance can be employed to reduce conduction loss.

For simplifying the analysis process of current stress of the presented converter operating in CCM, the current ripples of inductors and load  $R_L$  are neglected, the average current of inductors and load  $R_L$  are considered as  $I_{L1}$ ,  $I_{L2}$ ,  $I_{L11}$ , and  $I_{L21}$  and  $I_o$ , respectively. By applying the current-second balance principle on capacitors, the average value of current passing through diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  and inductors  $L_2$ ,  $L_{11}$ , and  $L_{21}$  are approximately the same as average output current  $I_o$ , we have

$$I_{D1} = I_{D11} = I_{D21} = I_{L2} = I_{L11} = I_{L21} = I_o \quad (17)$$

To simplify the analysis process, the components are considered as ideal. Therefore, the conversion efficiency of presented converter can approach 100%. Based on (4), average input current  $I_{L1}$  is given by

$$I_{L1} = I_o \frac{3D}{1-D} \quad (18)$$

As depicted in Fig. 4(a), the average current  $I_{S1}$  passing through switch  $S_1$  is obtained as

$$I_{S1} = (I_{L1} + I_{L2} + I_{L11} + I_{L21})D = I_o \frac{3D}{1-D} \quad (19)$$

The double-cells of presented SEPIC-TBC converter can be extended to include  $n$  basic cells, and hence

$$\begin{cases} I_{S1} = I_o \frac{(n+1)D}{1-D} \\ I_{L1} = I_o \frac{(n+1)D}{1-D} \\ I_{L11} = I_{L21} = \dots = I_{Ln1} = I_o \\ I_{D1} = I_{D11} = I_{D21} = \dots = I_{Dn1} = I_o \end{cases} \quad (20)$$

### C. Boundary Condition Mode

If the presented SEPIC-TBC converter operates in the boundary condition mode (BCM), it can be obtained that voltage conversion gain  $M_{CCM}$  will be equal to voltage conversion gain  $M_{DCM}$ . The boundary parameter  $\tau_B$  is found as (21) by using formulas (4) and (13).

$$\tau_B = \frac{(1-D)^2}{9} \quad (21)$$

The curve of boundary parameter  $\tau_B$  versus duty ratio is depicted in Fig. 8. If  $\tau$  is less than  $\tau_B$ , the presented converter operates in DCM condition, otherwise the converter operates in CCM condition.

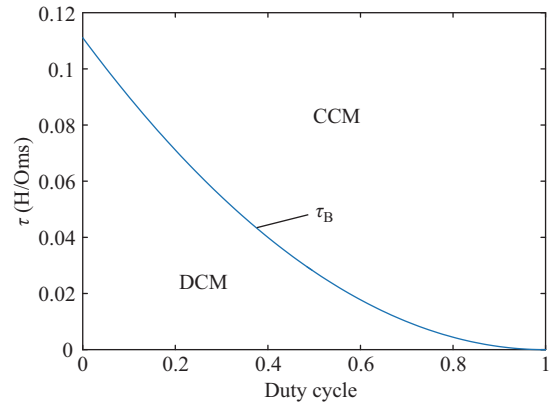


Fig. 8. Boundary condition of presented SEPIC-TBC converter operating in CCM and DCM.

A similar boundary condition mode analysis can be performed for presented SEPIC-CII converter with  $n$  basic cells, and the boundary mode is given by

$$\begin{cases} \tau_n \geq \tau_{Bn}, & \text{CCM} \\ \tau_n \leq \tau_{Bn}, & \text{DCM} \end{cases} \quad (22)$$

where  $\tau_n = \frac{2L_0 L}{(L+(n+1)L_0)R_L T_S}$  and  $\tau_{Bn} = \frac{(1-D)^2}{(1+n)^2}$ .

TABLE II  
COMPARISON OF THE SEPIC-CII CONVERTER WITH OTHER CONVERTERS

| Topology                 | SEPIC-CII converter         | Converter in [18] | Converter in [19]               | Converter in [28] | Cuk-derived step-up/down converter in [31]          | SEPIC           |
|--------------------------|-----------------------------|-------------------|---------------------------------|-------------------|-----------------------------------------------------|-----------------|
| Number of switches       | 1                           | 1                 | 1                               | 1                 | $2n - 1$                                            | 1               |
| Number of diodes         | $1 + n$                     | 3                 | 5                               | 3                 | $n$                                                 | 1               |
| Number of inductors      | $2 + n$                     | 3                 | 3                               | 4                 | 2                                                   | 2               |
| Number of capacitors     | $2 + 2n$                    | 5                 | 3                               | 6                 | $n + 1$                                             | 2               |
| Voltage gain             | $\frac{(n+1) \cdot D}{1-D}$ | $\frac{-3D}{1-D}$ | $-\left(\frac{D}{1-D}\right)^2$ | $\frac{3D}{1-D}$  | $\frac{nD}{1-D}$                                    | $\frac{D}{1-D}$ |
| Switch voltage stress    | $\frac{u_o}{(n+1)D}$        | $\frac{u_o}{3D}$  | $\frac{u_o}{D^2}$               | $\frac{u_o}{3D}$  | $\frac{mu_o}{(nD)}$<br>( $m = 1, 2, \dots, (n-1)$ ) | $\frac{u_o}{D}$ |
| Continuous input current | YES                         | NO                | YES                             | YES               | YES                                                 | YES             |

#### D. Comparison Between the Presented Converter and Other Converters

The properties contrast of the presented SEPIC-CII converter and some buck-boost converters with high step-up conversion gain are listed in Table II. Comparisons have involved voltage gain, components number and voltage stress, etc. In comparison with traditional SEPIC converters, the presented SEPIC-CII converter can acquire a higher voltage transfer ratio and reduce voltage stress across active components without extreme duty cycle. The common drawback of converters of [18], [19] is negative output voltage  $u_o$ . Besides, the converter in [18] has discontinuous input current, thus an auxiliary input filter is needed for some renewable energy applications.

Moreover, voltage stress across capacitors is high. In [19], the switches of converters suffer from high voltage stress. The characteristics of converter in [28] and presented converter with 2 basic cells are similar. However, compared to a converter with constant structure of [28], the presented SEPIC-CII converter can not only obtain larger voltage conversion ratio, but also reduce voltage stress on capacitors by adding its basic cells. The high step-up capacity of Cuk-derived step-up/down converter with expansion ability in [31] can be enhanced, but the number of switches is larger as  $n$  increases, thus the driver and control circuit are complex. Fig. 9 gives the relationship between voltage gain and duty cycle of the SEPIC-TBC converter and other converters.

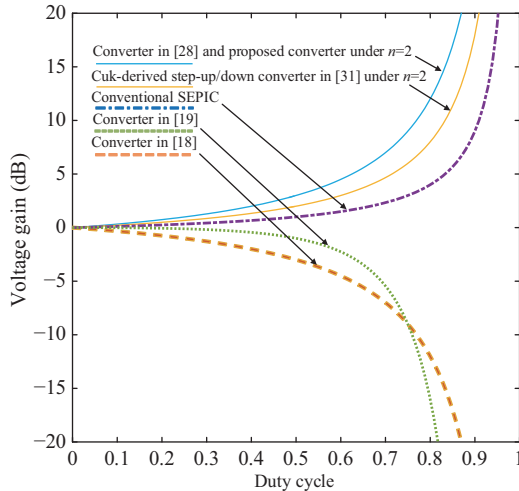


Fig. 9. Voltage gain versus duty cycle of various converters.

#### IV. EXPERIMENTAL RESULTS

A 300 W laboratory prototype was implemented to prove the theoretical analysis of the presented SEPIC-TBC converter operating in CCM, the photo is shown in Fig. 10. Typical specifications of the designed prototype are given in Table III. In this design of the prototype, the GaN transistor GS66508B from GaN Systems is used to operate the converter in 1 MHz frequency condition, thus the size of the inductors and capacitors components can be reduced significantly. In contrast with the converter of [30], the SEPIC-TBC converter presents higher power density. Fig. 11 shows the experimental results.

Figure 11(a) is the waveforms of the input voltage  $u_{in}$ , output voltage  $u_o$ , switch voltage stress  $u_{S1}$ , and drive signal  $u_{gs1}$ . As shown in this figure, when the voltage gain is about 8.3 with 73.5% duty cycle, output voltage  $u_o$  can be up to 400 V with 48 V input voltage, switch voltage stress is approximately 181 V. Experimental waveforms correspond

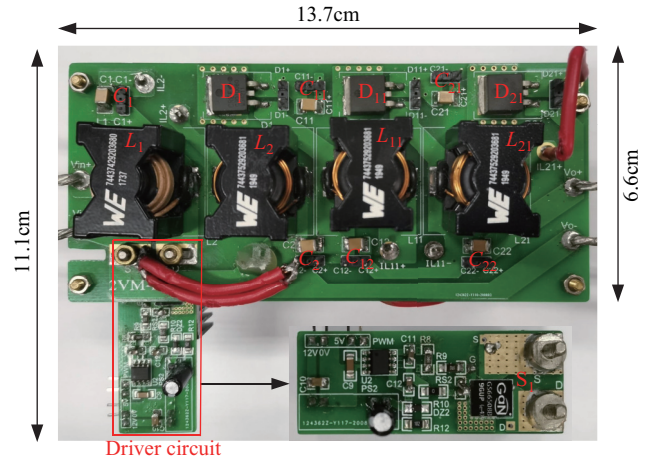


Fig. 10. Laboratory prototype of the SEPIC-TBC converter.

TABLE III  
PROTOTYPE SPECIFICATIONS OF THE CONVERTER

| Parameter                                | Values      |
|------------------------------------------|-------------|
| Input voltage ( $u_{in}$ )               | 48 V        |
| Output voltage ( $u_o$ )                 | 400 V       |
| Output power ( $P_o$ )                   | 300 W       |
| Switching frequency ( $f_s$ )            | 1 MHz       |
| Switch ( $S_1$ )                         | GS66508B    |
| Diodes ( $D_1, D_{11}, D_{21}$ )         | C3D10060    |
| Capacitors ( $C_1, C_2, \dots, C_{22}$ ) | 1 $\mu$ F   |
| Inductors ( $L_1$ )                      | 50 $\mu$ H  |
| Inductors ( $L_2, L_{11}, L_{21}$ )      | 100 $\mu$ H |

with the theoretical calculation. Voltage stress across diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  is close to 48 V, 133 V, and 133 V respectively, as demonstrated in Fig. 11(b), which agrees with (15). Figs. 10(c) and 11(d) illustrate the voltage waveforms of capacitors  $C_1$ ,  $C_2$ ,  $C_{11}$ ,  $C_{21}$ ,  $C_{12}$ , and  $C_{22}$ . Voltage across capacitor  $C_1$  is about 48 V, the voltage across other capacitors is the same and about 133 V, which agrees with the (7). Fig. 11(e) shows the current waveforms of inductors  $L_1$ ,  $L_2$ ,  $L_{11}$ , and  $L_{21}$ . The average value of current passing through inductor  $L_1$  reaches 6.25 A and it features low current ripple. The average value of current passing through inductors  $L_2$ ,  $L_{11}$ , and  $L_{21}$  is the same and about 0.75 A, which agrees with theoretical calculation.

Figure 12(a) depicts efficiency curve of designed prototype under different output powers. Maximum conversion efficiency can reach 93.8% at 275 W output power. The efficiency curve of designed prototype under different output voltages is given

in Fig. 12(b). Maximum conversion efficiency can reach 94.2% at 300 V output voltage.

Figure 13 illustrates the curve of duty cycle ( $D$ ) versus voltage gain ( $M$ ). As shown in this figure, the dotted line represents the theoretically calculated voltage gain, the solid line represents the experimentally measured voltage gain. Apparently, the experimental voltage gain value gradually drops below the value of theoretical result as  $D$  increases. The reason is that experimental result is largely influenced by experimental factors such as parasitic parameters, so the experimental voltage gain value of the presented SEPIC-TBC converter deviates from that of theoretical calculation.

## V. POWER DISSIPATION ANALYSIS

Power dissipation of the SEPIC-TBC converter mainly consists of conduction and switching dissipation of switches,

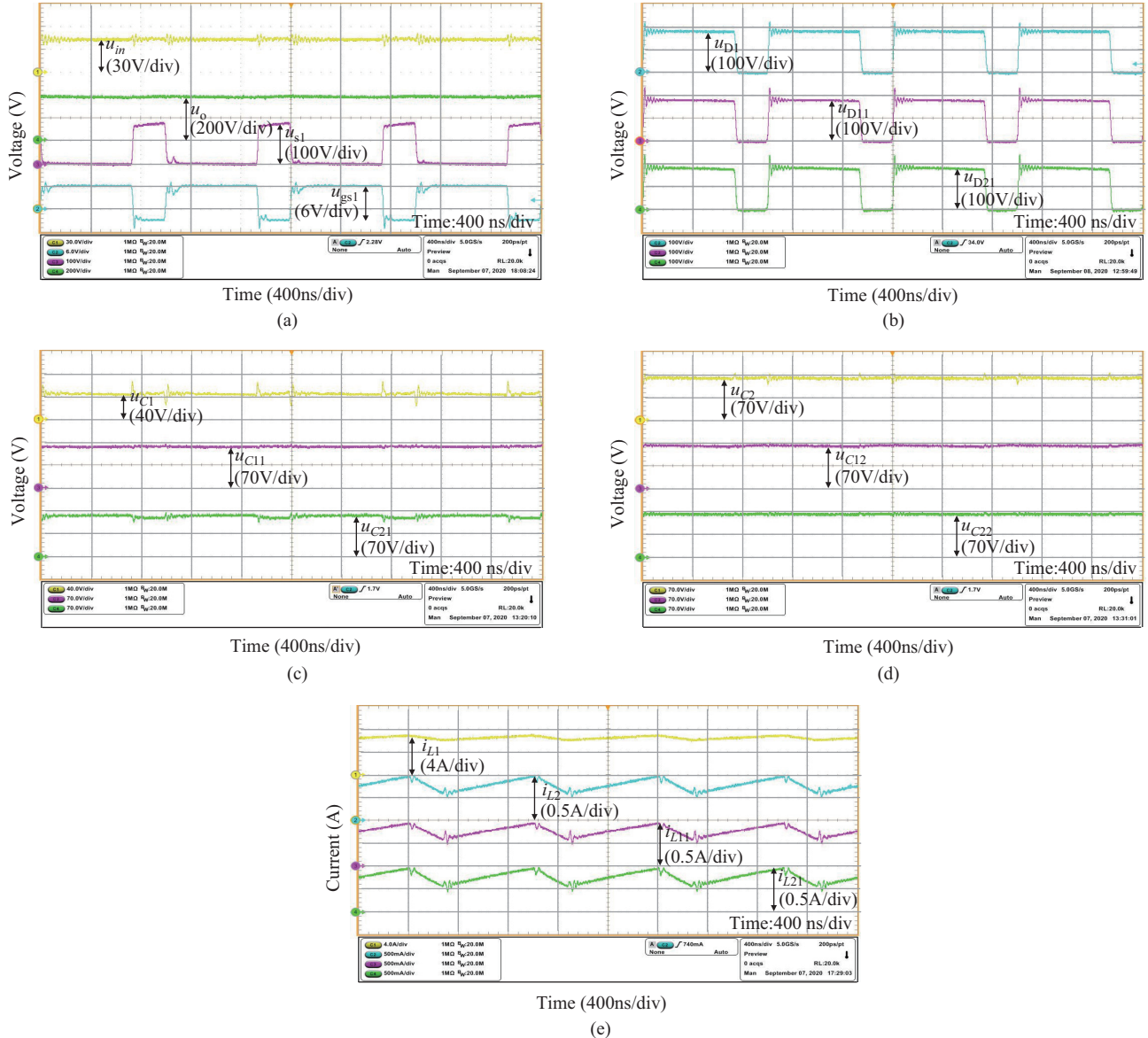


Fig. 11. Experimental results of the designed prototype. (a)  $u_{gs1}$ ,  $u_{in}$ ,  $u_{s1}$ ,  $u_o$ . (b)  $u_{D1}$ ,  $u_{D11}$ ,  $u_{D21}$ . (c)  $u_{C1}$ ,  $u_{C11}$ ,  $u_{C21}$ . (d)  $u_{C2}$ ,  $u_{C12}$ ,  $u_{C22}$ . (e)  $i_{L1}$ ,  $i_{L2}$ ,  $i_{L11}$ ,  $i_{L21}$ .

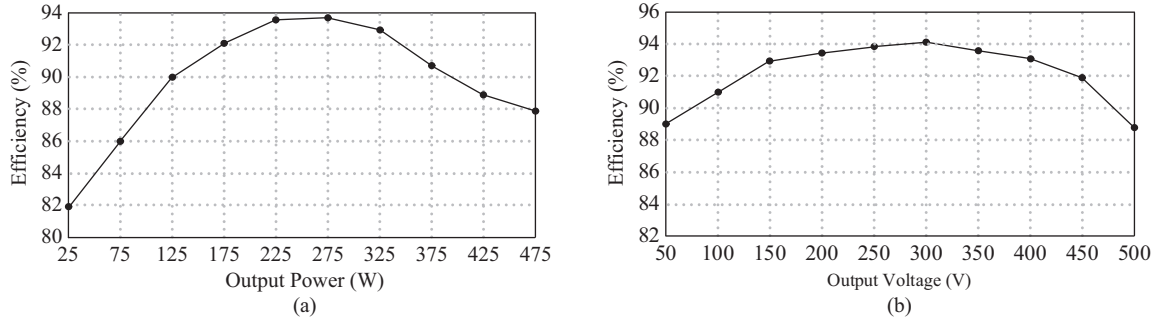


Fig. 12. Efficiency curve of the designed prototype. (a) Efficiency curve under different output power. (b) Efficiency curve under different output voltage.

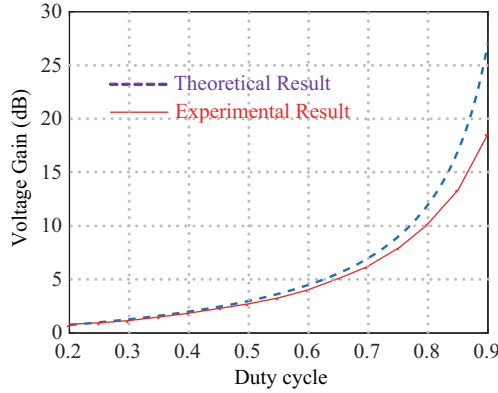


Fig. 13. The duty cycle versus the voltage gain for the presented SEPIC-TBC converter.

diodes conduction dissipation, and inductors conduction dissipation. For simplifying the mathematical analysis process of loss, the current ripple of the inductors, and voltage ripple of the capacitors are ignored. The loss of each part can be obtained by calculation according to prototype parameters listed in Table III. Detailed theoretical loss analysis are described as follows.

Switch conduction dissipation is given by

$$P_{s\text{-cond}} = I_{s\text{-rms}}^2 R_{\text{dson}} = \frac{9D}{(1-D)^2} I_o^2 R_{\text{dson}} = 2.6 \text{ W} \quad (23)$$

where  $R_{\text{dson}}$  is the on-state resistance of switch,  $I_{s\text{-rms}}$  is the RMS value of the current passing through switch.

Switch turn-on dissipation is given by

$$P_{\text{on}} = \frac{u_s i_{\text{on}} t_{\text{t-on}}}{2T_s} \quad (24)$$

where  $t_{\text{t-on}}$  is the time interval of the turn-on transition of switch,  $u_s$  is switch voltage, and  $i_{\text{on}}$  represents current passing through switch during switch turn on.

Switch turn-off dissipation is given by

$$P_{\text{off}} = \frac{u_s i_{\text{off}} t_{\text{t-off}}}{2T_s} \quad (25)$$

where  $t_{\text{t-off}}$  is the time interval of the turn-off transition of switch, and  $i_{\text{off}}$  represents current passing through switch during switch turns off.

Total switching dissipation of switch can be given by

$$P_{s\text{-w}} = P_{\text{on}} + P_{\text{off}} = \frac{u_o I_o (t_{\text{t-on}} + t_{\text{t-off}})}{2D(1-D)T_s} = 6.86 \text{ W} \quad (26)$$

Diode conduction dissipation is given by

$$P_{\text{d-cond}} = V_F I_d \quad (27)$$

where  $V_F$  denotes the forward voltage drop of the diode, and  $I_d$  is the average value of current passing through diode.

Total conduction dissipation of diodes  $D_1$ ,  $D_{11}$ , and  $D_{21}$  can be calculated as follows:

$$P_{\text{d-tot}} = 3V_F I_d = 2.25 \text{ W} \quad (28)$$

Inductor conduction dissipation is expressed as follows:

$$P_{L\text{-cond}} = I_{L\text{-rms}}^2 R_L \quad (29)$$

where  $R_L$  is the ESR value of inductor, and  $I_{L\text{-rms}}$  represents the RMS value of current passing through inductor.

Total conduction dissipation of inductors  $L_1$ ,  $L_2$ ,  $L_{11}$ , and  $L_{21}$  can be calculated by the following expression:

$$P_{L\text{-tot}} = I_{L1\text{-rms}}^2 R_{L1} + 3I_{L2\text{-rms}}^2 R_{L2} = 2.2 \text{ W} \quad (30)$$

The other losses includes capacitor loss, drive loss and PCB line conduction loss, which will be given an estimated values. The value can be calculated as follows:

$$P_{\text{other}} = 2 \text{ W} \quad (31)$$

Based on aforementioned theoretical calculation, power dissipation distribution of the presented converter is illustrated in Fig. 14 at 300 W output power and 400 V output voltage. As can be concluded from the pie chart, 43.2% dissipation of total power dissipation is caused by the switch turn-on and turn-off transition, which is the major dissipation. Conduction

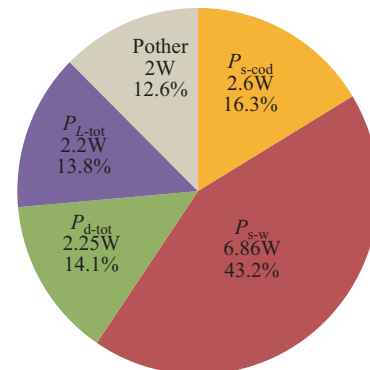


Fig. 14. Theoretical power dissipation distribution of the presented converter.

dissipation of switch and diodes contributes 30.4% of total dissipation. Inductors conduction dissipation contributes 13.8% of total dissipation and remaining dissipation caused by other parasitic elements contributes 12.6% of total dissipation.

## VI. CONCLUSION

This paper proposes a novel family of coat circuits for basic SEPIC converters. A 1-MHz 300-W laboratory prototype is designed to validate the theoretical analysis of the presented SEPIC-TBC converter.

1) The presented general SEPIC converters with coat circuit have these merits of large voltage conversion ratio, low switch and diodes voltage stress, simply driver and control circuit, and low input current ripple.

2) The presented SEPIC-TBC converter has better performance in power density by using a GaN device.

3) The presented family of modified SEPIC converters can achieve lower voltage and current stress on the capacitors, which can effectively reduce selection restriction and cost of components.

4) The presented family of converters is more feasible to industrial applications like PV power generation and FC systems.

## REFERENCES

- [1] A. Mirzaee and J. S. Moghani, "Coupled inductor-based high voltage gain DC–DC converter for renewable energy applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7045–7057, Jul. 2020.
- [2] S. Habib, M. M. Khan, F. Abbas, A. Ali, M. T. Faiz, F. Ehsan, and H. J. Tang, "Contemporary trends in power electronics converters for charging solutions of electric vehicles," *CSEE Journal of Power and Energy Systems*, vol. 6, no. 4, pp. 911–929, Dec. 2020.
- [3] P. Cheng, H. Kong, C. Wu, and J. Ma, "Integrated Configuration and Control Strategy for PV Generation in Railway Traction Power Supply Systems," *CSEE Journal of Power and Energy Systems*, vol. 8, no. 6, pp. 1603–1612, Nov. 2022.
- [4] A. A. Desai, and S. Mikkili, "Modeling and Analysis of PV Configurations to Extract Maximum Power Under Partial Shading Conditions," *CSEE Journal of Power and Energy Systems*, vol. 8, no. 6, pp. 1670–1683, Nov. 2022.
- [5] Y. Zhang, H. Y. Liu, J. Li, M. Sumner, and C. L. Xia, "DC–DC boost converter with a wide input range and high voltage gain for fuel cell vehicles," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4100–4111, May 2019.
- [6] M. E. Azizkandi, F. Sedaghati, H. Shayeghi, and F. Blaabjerg, "Two- and three-winding coupled-inductor-based high step-up DC–DC converters for sustainable energy applications," *IET Power Electronics*, vol. 13, no. 1, pp. 144–156, Jan. 2020.
- [7] I. U. Nutkani, L. Meegahapola, A. L. P. Chiang, and F. Blaabjerg, "Autonomous power management for interlinked AC–DC microgrids," *CSEE Journal of Power and Energy Systems*, vol. 4, no. 1, pp. 11–18, Mar. 2018.
- [8] B. X. Zhu, Z. H. Wei, Y. Chen, H. Wang, and D. M. Vilathgamuwa, "Multiple input-terminal voltage multiplier circuit," *IEEE Transactions on Industry Applications*, vol. 56, no. 5, pp. 5075–5082, Sep./Oct. 2020.
- [9] T. J. Liang, J. H. Lee, S. M. Chen, J. F. Chen, and L. S. Yang, "Novel isolated high-step-up DC–DC converter with voltage lift," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1483–1491, Apr. 2013.
- [10] Q. F. Wu, Q. Wang, J. L. Xu, and Z. L. Xu, "Active-clamped ZVS current-fed push–pull isolated dc/dc converter for renewable energy conversion applications," *IET Power Electronics*, vol. 11, no. 2, pp. 373–381, Feb. 2018.
- [11] K. Yari, S. H. Shahalami, and H. Mojallali, "High step-up isolated dc–dc converter with single input and double output and soft-switching performance for renewable energy applications," *IET Power Electronics*, vol. 12, no. 11, pp. 2942–2952, Sep. 2019.
- [12] S. Sathyan, H. M. Suryawanshi, B. Singh, C. Chakraborty, V. Verma, and M. S. Ballal, "ZVS–ZCS high voltage gain integrated boost converter for DC microgrid," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 6898–6908, Nov. 2016.
- [13] H. Ardi, A. Ajami, and M. Sabahi, "A novel high step-up DC–DC converter with continuous input current integrating coupled inductor for renewable energy applications," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1306–1315, Feb. 2018.
- [14] S. Vighetti, J. P. Ferrieux, and Y. Lembeye, "Optimization and design of a cascaded DC/DC converter devoted to grid-connected photovoltaic systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2018–2027, Apr. 2012.
- [15] P. Saadat and K. Abbaszadeh, "A single-switch high step-up DC–DC converter based on quadratic boost," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7733–7742, Dec. 2016.
- [16] A. M. S. S. Andrade, L. Schuch, and M. L. da Silva Martins, "Analysis and design of high-efficiency hybrid high step-up DC–DC converter for distributed PV generation systems," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3860–3868, May 2019.
- [17] M. R. Banaei, H. Ardi, and A. Farakhor, "Analysis and implementation of a new single-switch buck-boost dc/dc converter," *IET Power Electronics*, vol. 7, no. 7, pp. 1906–1914, Jul. 2014.
- [18] M. R. Banaei and H. A. F. Bonab, "A novel structure for single-switch nonisolated transformerless buck–boost DC–DC converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 198–205, Jan. 2017.
- [19] N. Zhang, G. D. Zhang, K. W. See, and B. Zhang, "A single-switch quadratic buck–boost converter with continuous input port current and continuous output port current," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4157–4166, May 2018.
- [20] S. Lee, P. Kim, and S. Choi, "High step-up soft-switched converters using voltage multiplier cells," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3379–3387, Jul. 2013.
- [21] Z. Waradzyn, R. Stala, A. Mondzik, A. Penczek, A. Skala, and S. Pirog, "Efficiency analysis of MOSFET-based air-choke resonant DC–DC step-up switched-capacitor voltage multipliers," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8728–8738, Nov. 2017.
- [22] B. X. Zhu, L. L. Ren, X. Wu, and K. Song, "ZVT high step-up DC/DC converter with a novel passive snubber cell," *IET Power Electronics*, vol. 10, no. 5, pp. 599–605, Apr. 2017.
- [23] A. Rajaei, R. Khazan, M. Mahmoudian, M. Mardaneh, and M. Gitizadeh, "A dual inductor high step-up DC/DC converter based on the Cockcroft–Walton multiplier," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9699–9709, Nov. 2018.
- [24] B. X. Zhu, Q. D. Zeng, Y. Chen, Y. H. Zhao, and S. Liu, "A dual-input high step-up DC/DC converter with ZVT auxiliary circuit," *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 161–169, Mar. 2019.
- [25] H. Ardi and A. Ajami, "Study on a high voltage gain SEPIC-based DC–DC converter with continuous input current for sustainable energy applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10403–10409, Dec. 2018.
- [26] S. Hasanpour, A. Baghrmian, and H. Mojallali, "A modified SEPIC-based high step-up DC–DC converter with quasi-resonant operation for renewable energy applications," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3539–3549, May 2019.
- [27] M. Heydari, H. Khoramikia, and A. Fatemi, "High-voltage gain SEPIC-based DC–DC converter without coupled inductor for PV systems," *IET Power Electronics*, vol. 12, no. 8, pp. 2118–2127, Jul. 2019.
- [28] M. R. Banaei and S. G. Sani, "Analysis and implementation of a new SEPIC-based single-switch buck–boost DC–DC converter With continuous input current," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10317–10325, Dec. 2018.
- [29] S. S. Gao, Y. J. Wang, Y. S. Guan, and D. G. Xu, "A high-frequency high voltage gain modified SEPIC with integrated inductors," *IEEE*

*Transactions on Industry Applications*, vol. 55, no. 6, pp. 7481–7490, Nov./Dec. 2019.

- [30] B. X. Zhu, F. Ding, and D. M. Vilathgamuwa, “Coat circuits for DC-DC converters to improve voltage conversion ratio,” *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3679–3687, Apr. 2020.
- [31] M. Abbasi, E. Babaei, and B. Tousi, “New family of non-isolated step-up/down and step-up switched-capacitor-based DC-DC converters,” *IET Power Electronics*, vol. 12, no. 7, pp. 1706–1720, Jun. 2019.



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